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DEVELOPMENT OF SHORT GATE FET'S

FINAL REPORT
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JULY 1985

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HOWARD UNIVERSITY
ELECTRICAL ENGINEERING
SOLID-STATE ELECTRONICS GROUP
WASHINGTON, D.C.20059

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Introduction

The primary research objective of this project was to investigate the possibilities of improved performance in the "standard" GaAs field effect transistor structures. A secondary objective was to determine the extent to which Deep UV Lithography could be used as a technique to produce high resolution geometries. At this point in time we have succeed in the second endeavor and can now routinely produce 0.5 micron gate geometries with Deep UV lithography and occasionaly we have produced sub .25 micron structures. Using this technology we have produced devices with "state of the art ", electrical characteristics. Toward the end of this reporting period and into the last term of the contract we are investigating a novel structure to try and increase the output conductance of our devices. As an aside we have investigate the annealing of undoped epitaxial material and have obtained some interesting resuls which are the subject of our first Phd. thesis.

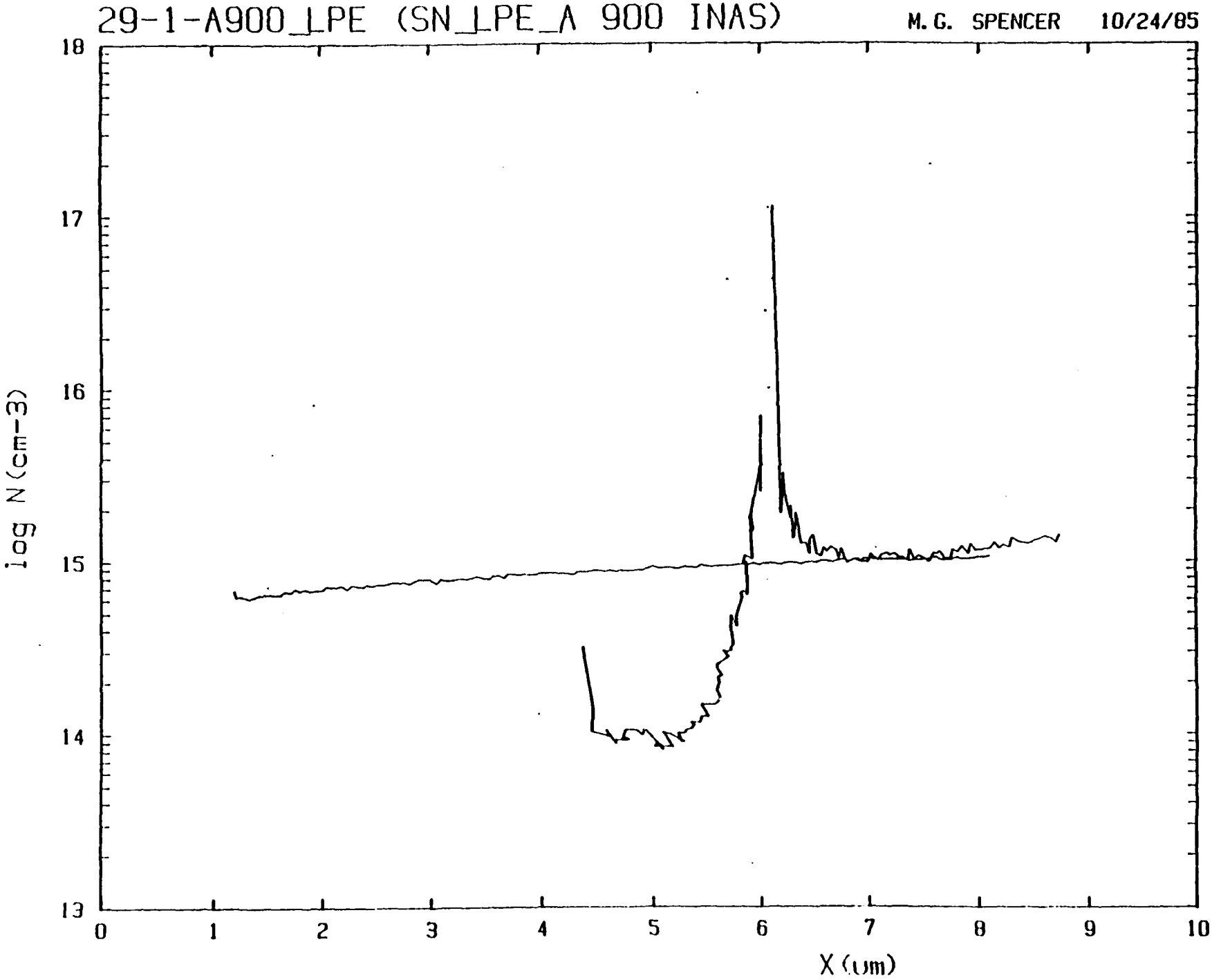
Status of Research

The status of our devices and Deep UV Lithography research is summarized in the attached chapters of the masters thesis of Leary Myers .

In the experiments on annealing of epitaxial material we have found that even in thick LPE material out diffusion of substrate (see figure 1) impurities can be major problem. This out diffusion seems to occur regardless of the magnitude of the As overpressure (ie. anealing using GaAs as a source of As or InAs as a source of As). Curiously to date we have not observed such on MBE samples annealed. We are trying to explain these results in terms of the stociometry differencies in the respective epitaxial layers.

We are conducting experiments to attempt to improve the output conductance of FET's by inverting the structure (see Fig 2). In this structure the output conductance will be increased becuse of a more favorable geometry. Initial results using "makeshift masks" shows that the output conductance in long gate devices devices is 1500 ohms-mm.

We have finished characterizion of our MBE material (Fig 3). We found that sintering the Si source resulted in greatly improved doping uniformity. We are now concentrationg on the growth of GaAlAs and anticipate fabricating some HEMPT (modulation doped) devices before the end of the contract.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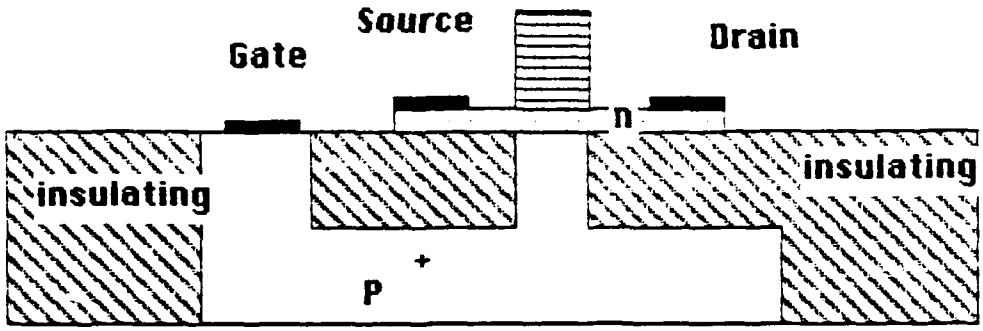
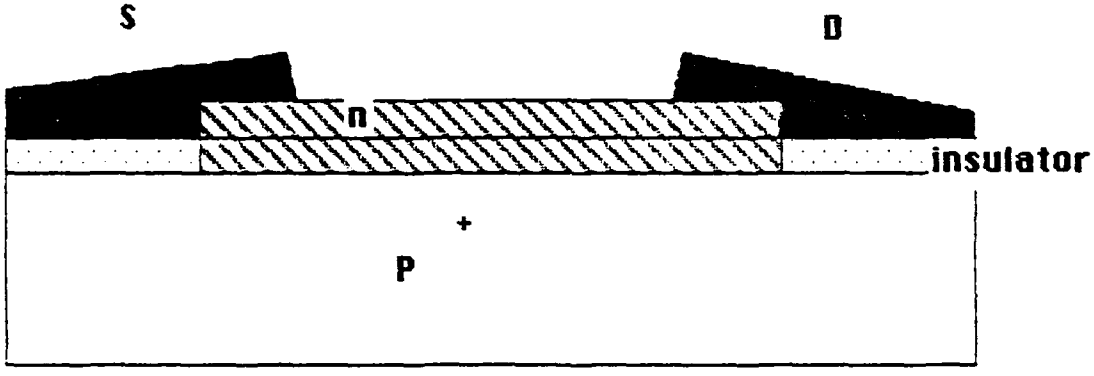
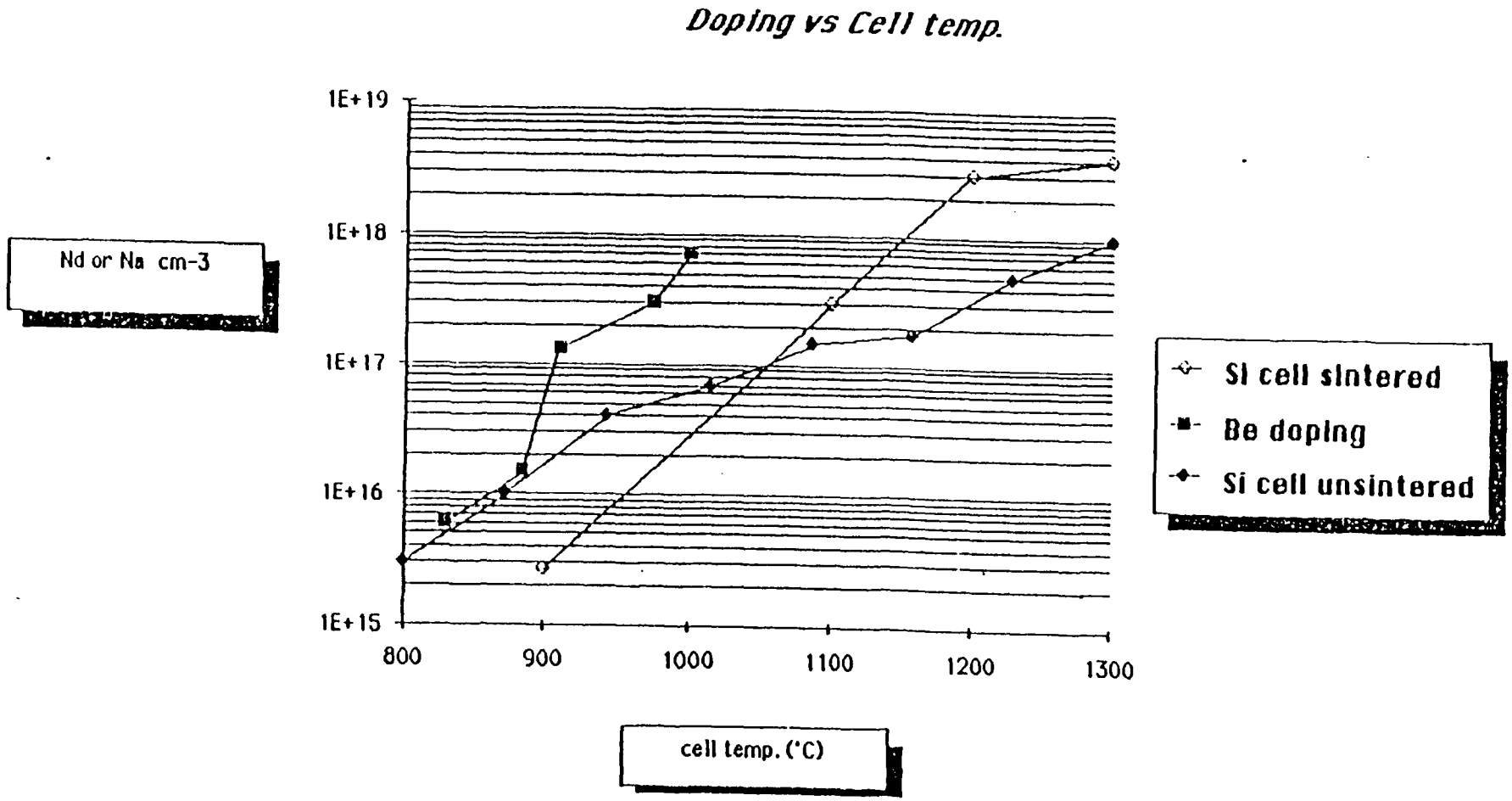




Schematic of Inverted Fet structure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1E+17
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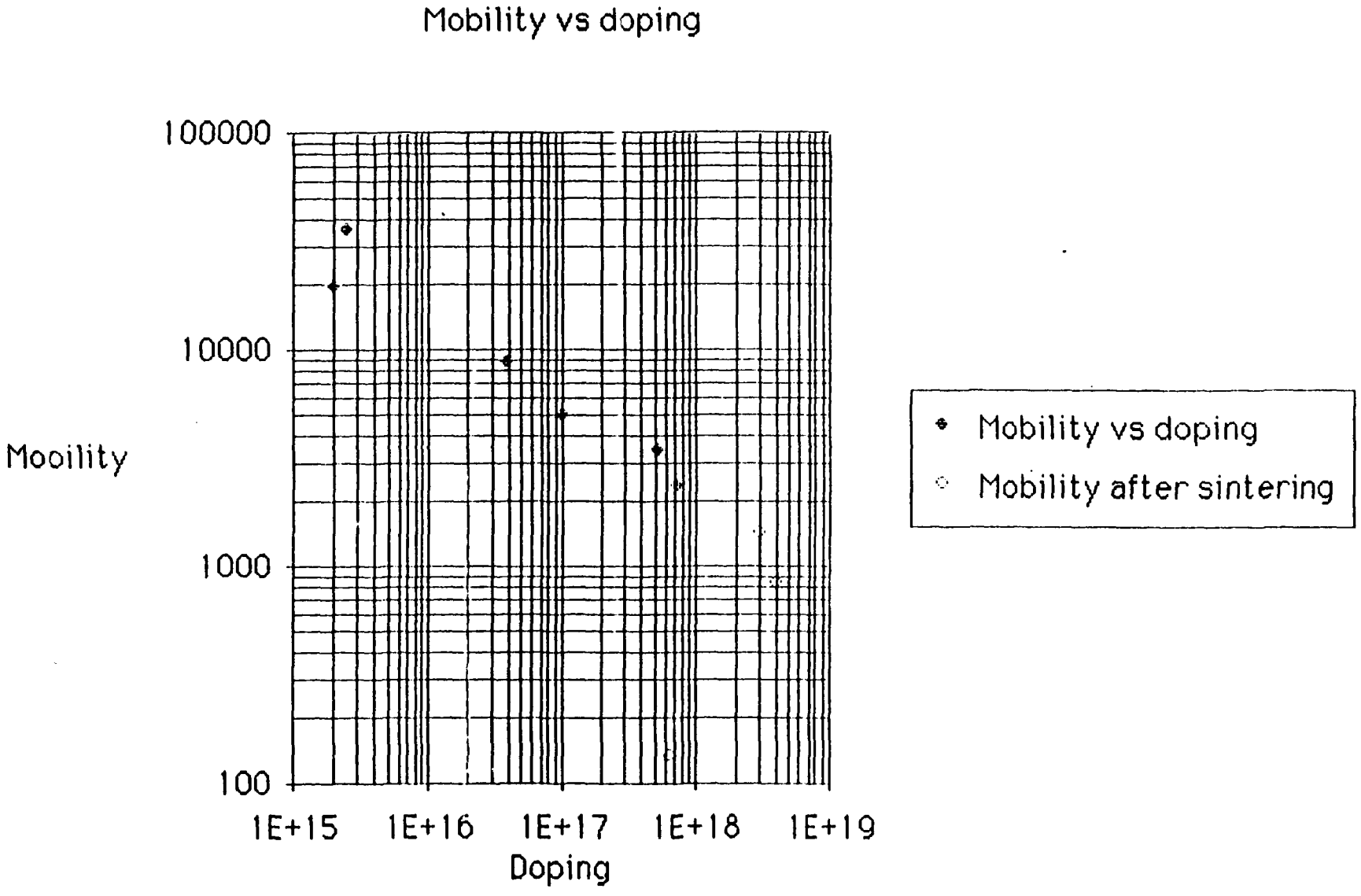
Si cell unsintered

Figure 5


Mobility vs doping
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1E+15
1E+16
1E+17
1E+18
1E+19
Doping
Mobility vs doping
Mobility after sintering

Figure 6

CHAPTER III

DEVICE FABRICATION

In an attempt to fabricate devices with sub-micron geometries, Deep Ultra Violet (DUV) contact lithography is utilized. The availability of a UV source in the 220-240 nm wavelength range (DUV) enables the achievement of feature sizes of less than 0.5 micron. In practice the minimum usable line width, W_L, reproducible by DUV is given by the expression $W_W = 15 (\lambda s/200)^{1/2}$ where λ is the wavelength of the radiation and S is the separation of the mask and the bottom of the photoresist. In this study, a Hybrid Technology Group (HTG) Model 345-5....aligner was used. The HTG DUV aligner is equipped with 500 watt Hg-Xe lamp capable of emitting radiation in the 220-240 nm range. The reflective and refractive elements, in the optical column, are ineffective filters of wavelengths in the 400 nm range. It is therefore necessary to use photoresists such as PMMA which are sensitive to wavelengths above 260 nm. The maximum intensity as measured by a HTG Model 100 probe is 22.0 mW per cm^2 for this aligner. Line widths as small as 0.25 microns

have been produced using this aligner using the vacuum contact mode.

In trying to fabricate sub-micron geometries, wafer topography is essential for high resolutions. In this work a double layer resist structure is utilized. The layers are PMMA and a copolymer P(MMA-CO-MAA). The copolymer is a thick bottom resist layer used to planarize the surface while PMMA is used as a thin imaging layer for high resolution. In addition to planarizing the surface the copolymer allows formation of a "lip structure" to provide an easy lift-off process.

The masks used in the processing, consist of Chromium on quartz patterned by direct write E-beam at the Submicron Center at Cornell University. Quartz is essential for DUV lithography since conventional glass plates do not transmit wavelengths below 300 nm. In addition quartz has low coefficient of expansion. All the wafers were ion-implanted by vendors ~~sources~~ and annealed in house.

A. Gate Definition

This is the most involved process in fabricating the FET. Utmost importance is placed on the cleanliness of the wafer's surface since virtually any foreign particle on the wafer will be of comparable size to the gate length. A standard clean is performed on the wafer and this includes washing the wafer in FL70 detergent, degreasing in boiling TCE for 3 minutes and rinsing in Acetone. The wafer is then put in Methanol and placed in an ultrasonic bath, to remove foreign particles, for five minutes. Finally the wafer is dipped in a HCL:Methanol 1:1 bath for 30 seconds, rinsed in deionized (DI) water and blown dry by nitrogen. The wafer is then baked out at 200°C for twenty minutes to remove any remaining water. Better adhesion of the photoresist to the wafer surface results when there is a sheet-off effect.

Copolymer is spun on at 2500 r.p.m. for one minute to give a layer 4000 Angstroms (A°) thick. The thickness of resist is ascertained by Dektak measurements. It is then baked at 170°C for 45 minutes to remove the solvents. Four percent PMMA is then spun on at 3000 r.p.m. for one minute

resulting in a layer 2500 A° thick. The wafer is again baked at 160°C for one hour.

In order to achieve good resolution, it is absolutely necessary to maintain intimate contact between the mask and the photoresist. Two steps were used. (1) Removal of the photoresist at the edge of the wafer and (2) a strip of rubber is placed beneath the wafer to aid in planarizing the wafer. To ascertain the kind of contact a clear quartz plate the same size as the mask was used. The wafer was observed under vacuum contact conditions through the clear plate. Areas of intimate contact corresponded to darkened regions. Excellent correlation between these contact areas and production of high quality lines was observed. After rotating and translating the wafer to optimize the darkened regions, the quartz plate is replaced by the actual mask. To achieve dark regions over a large percentage of the wafer has proven to be extremely difficult. The rubber placed at the

bottom of sample has helped considerably in obtaining darkened regions. The use of the rubber platform has greatly enhanced the production of submicron lines.

We have found that at a dose of 19.8 mW/per square cm for 6 minutes was adequate. The exposed resist is first developed in a two to one solution of propanol to toluene to remove the exposed PMMA. The second developer is a solution of ethoxy ethyl acetate (ECA) diluted in ethanol (1:10) to remove the copolymer. To ensure complete removal of the exposed resist, the wafer is placed in a O_2 plasma in a barrel plasma reactor. The calibrated etch rate for PMMA and the copolymer is shown in Figure 16. The developed photo resist with the lift of lip structure is shown in Figure 17.

Two thousand Angstroms of Titanium (Ti) are deposited along with 2000 A° of Au for the gate metallization, to create a total height of 0.4 microns. It is our experience that 2000 A° of Ti are necessary to provide adequate protection of the gate Schottky-barrier during alloying of the ohmic

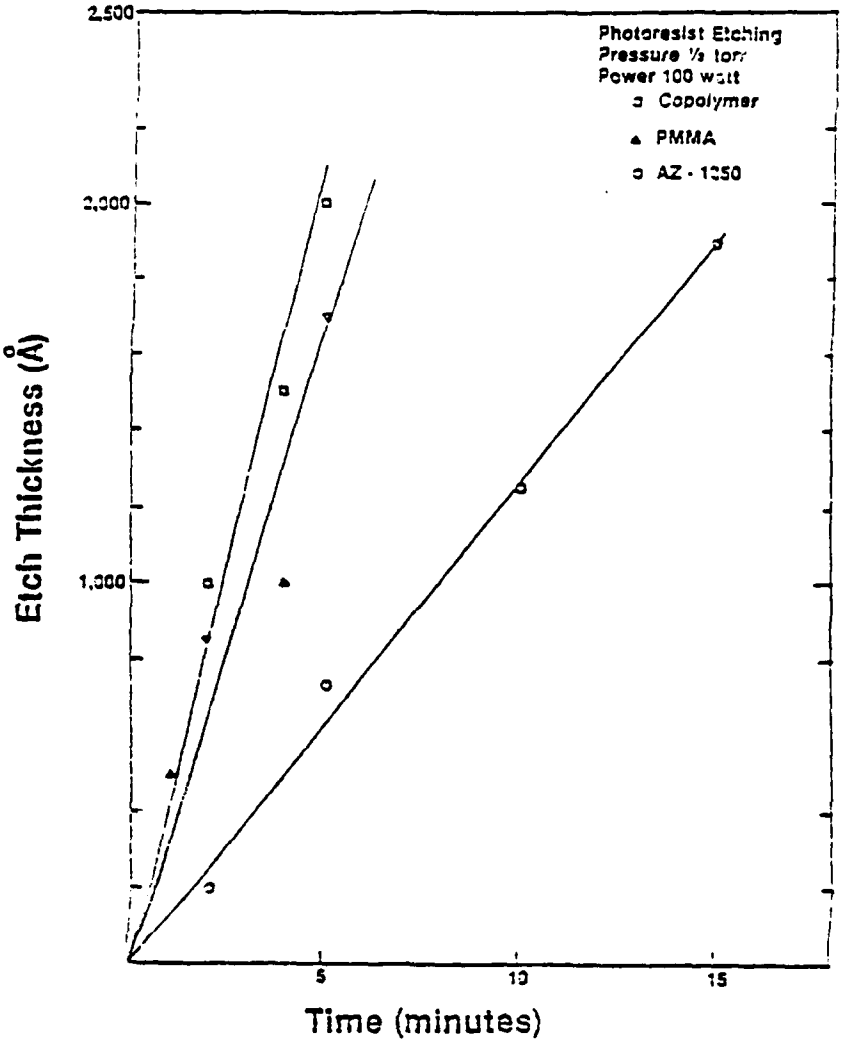


Figure 16: Calibration of resist etch rate.

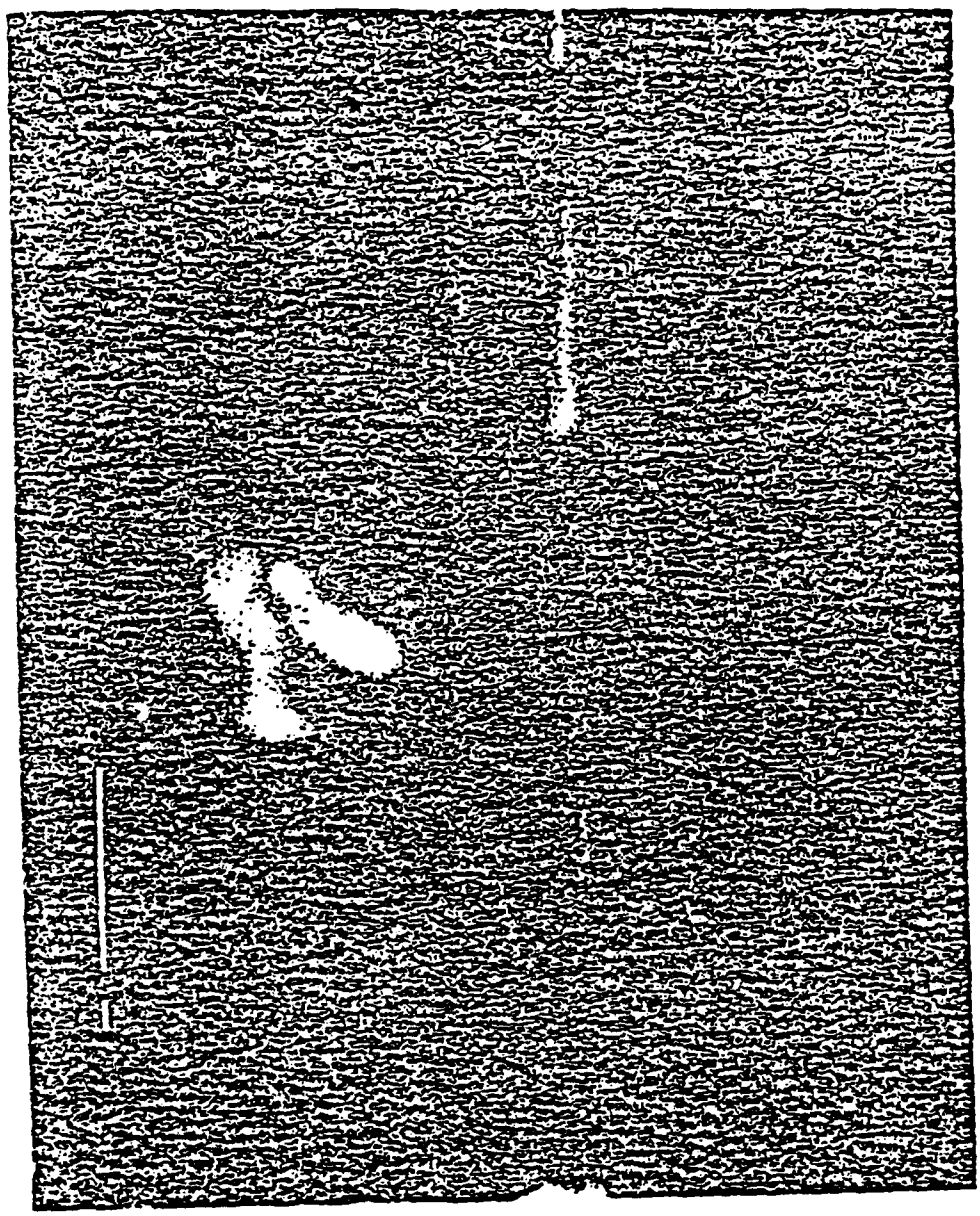


Figure 17: Lift-off "lip"

contacts. Figures 18, 19 and 20 are actual pictures of the better gate lift off.

B. Mesa Definition

To isolate devices on the wafer, the standard mesa etch technique was used. This method is done using AZ1470 resist and a KN5 aligner.

The resist is spun on at 4000 r.p.m. to give a 1.2 micron layer. After the removal of resist on the wafer edges, the mesa is aligned and wafer is exposed. To harden the resist covering the mesa, it is post baked for 20 minutes after development. An etch made from Ammonium Hydroxide, 30% Hydrogen Peroxide and DI water in the ratio 40:1:1 was found to serve our purposes best. The etch rate is 1000 A^{o} every 18 secs. From the doping, N_D versus depth, d, profile, the thickness of the active layer is determined. A typical mesa height is 3000A^{o}. To ensure complete isolation of the wafer surface that was etched, the surface is checked by a two point probe before the resist is removed by Acetone.

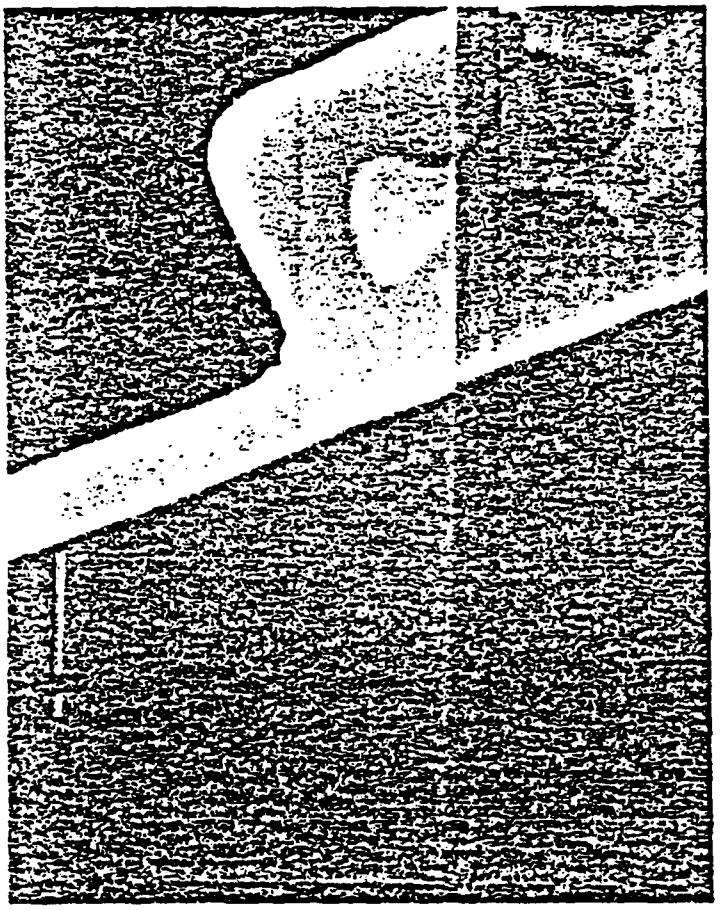


Figure 18: Gate metallization.

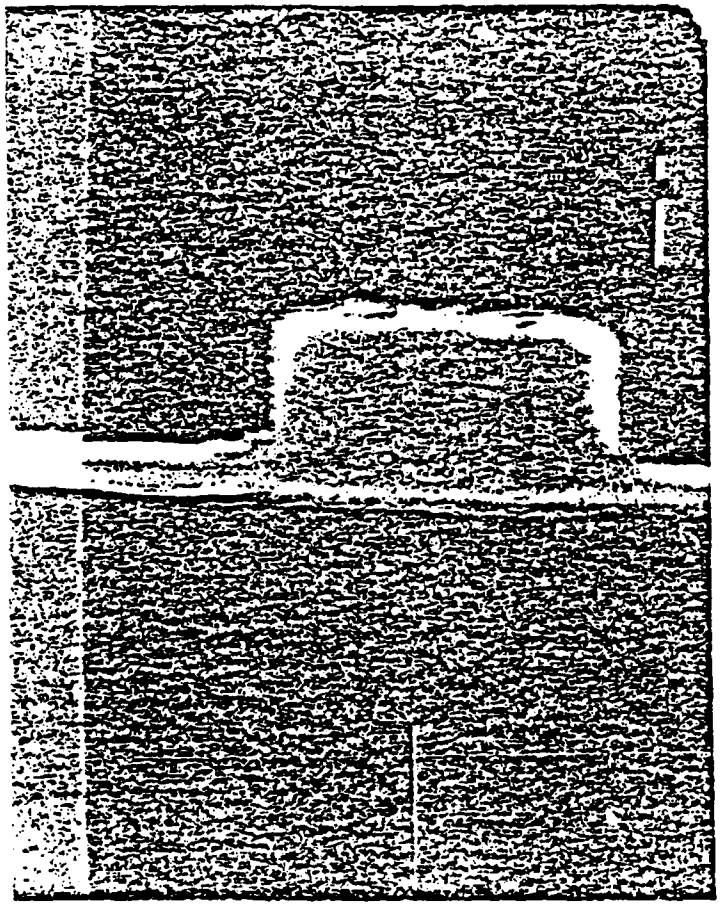


Figure 19: Gate metallization

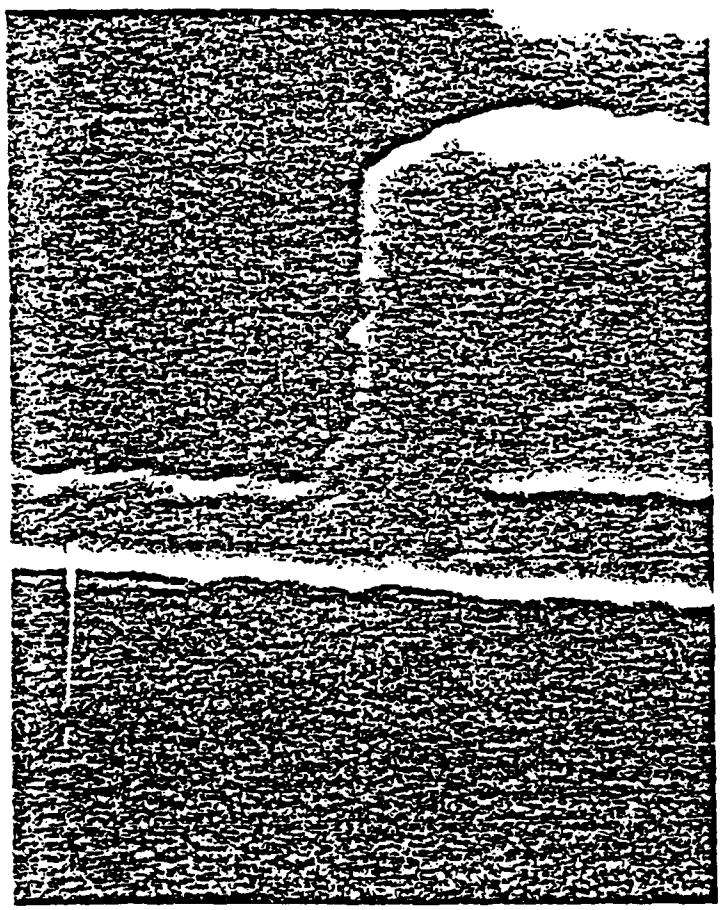


Figure 20: Gate metallization

C. Source and Drain Ohmic Contacts

After cleaning the wafer by Acetone followed by Methanol squirts and a DI water wash AZ 1450B is spun on to give a layer 0.4 microns thick. Following the same procedure, holes are opened for the source/drain metallization. Four hundred Angstorms of Gold Germanium (AuGe) is deposited by thermal evaporation, followed by one thousand Angstroms of Gold by E-beam evaporation. These contacts are alloyed at 450°C to form ohmic contacts. Figure 21 and 22 show pictures of these contacts. There is a noticeable "balling up" of the ohmic contacts during the alloying process. The introduction of Nickel into the AuGe reduces this effect. Successfully alloyed ohmic contacts have saturation currents of 30-35 mA at about 1.5V for the ion implanted layers.

D. Gate Pad Definition

In order to make electrical contact to the gate of the FET, with minimum parasitic capacitance, a gold metal pad is positioned on the

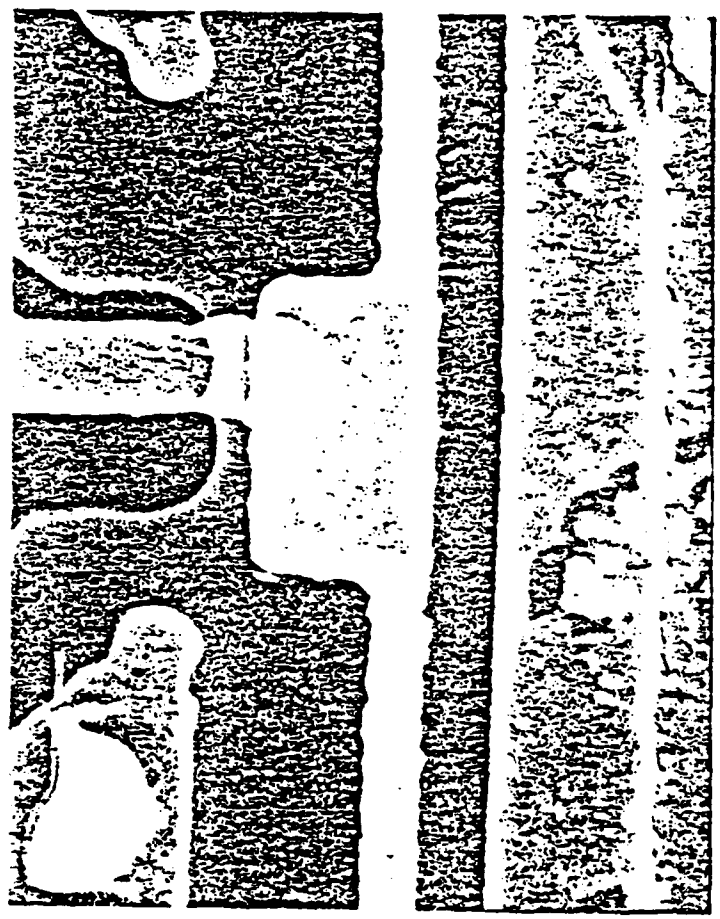


Figure 21: Scanning electron micrographs of completed FET calibration mark is one micron.

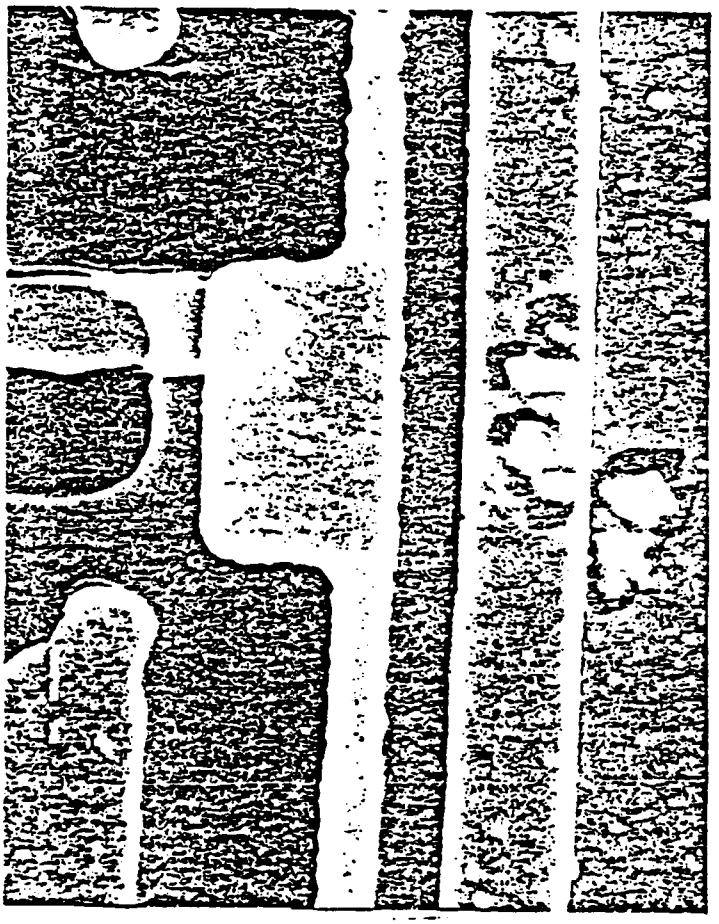


Figure 22: Scanning electron micrographs of completed FET. calibration mark is one micron.

substrate with a thin connecting strip touching the gate.

To achieve this, AZ 1450B is again used and a similar exposure/development process as the one used for the source/drain contacts definition is employed. Metallization is by E-beam evaporation of 1000A° of Gold. Figures 23, 24 and 25 are pictures of the completed FET.

Figure 23: Pictures of completed FET magnification is 1000.

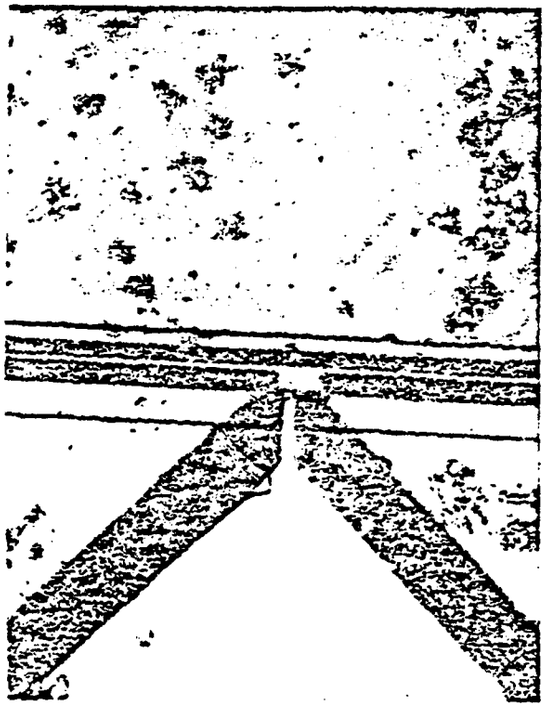


Figure 24: Pictures of completed FET
magnification is 1000.

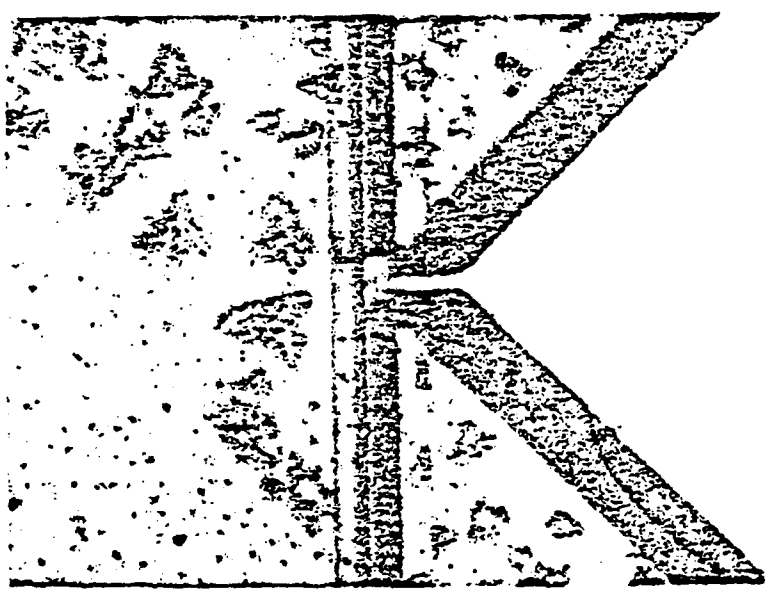


Figure 25: Pictures of completed FFT magnification is 1000.

CHAPTER IV

RESULTS

In this chapter results obtained from dc measurements of representative devices will be presented in tabular form. Pictures of the device I-V characteristics are also shown.

The dc parameters measured are

(1) Ideality factor, n

(2) Built-in gate barrier, V_{bi} (volts)

(3) Breakdown voltage, V_{br} (volts)

(4) Source resistance, R_s (ohms)

(5) Drain resistance, R_D (ohms)

(6) Pinch off voltage, V_p (volts)

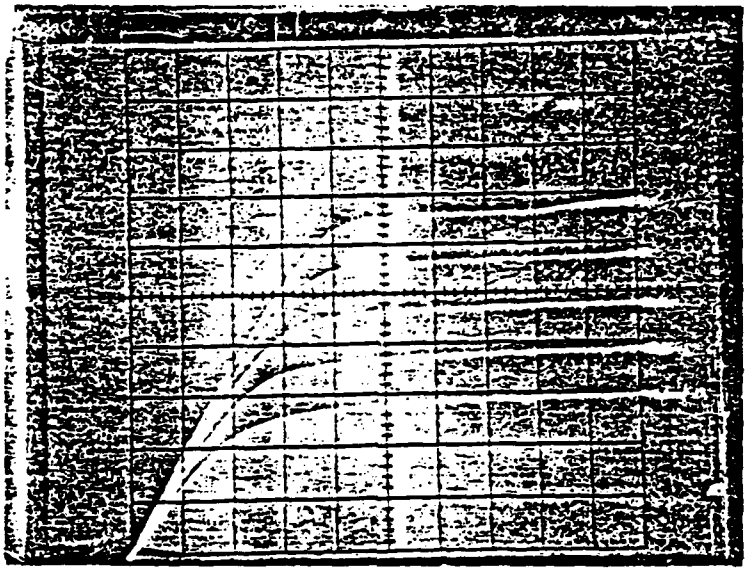
(7) Transconductance, g_m (milliseimens per millimeter)

(8) Gate length, L_g (microns)

The mask level defining the date has resolutions of 0.25, 0.5 and 0.75 microns. The vast majority of gates were 0.5 and 0.75 microns. Gate lengths of 0.25 microns have not been reproducible with any consistency. Figures 26 and 27 are I-V characteristics of the source-drain and gate for some of the better devices. For the better devices, the doping concentration was approximately $N_D = 1.2 \times 10^{17}$ per cm^3.

The gate width, Z was 150 microns and the separation between source and drain was 5 microns. Using Pucel's theoretical calculations (10) the value obtained for transconductace was, g_m = 157.13 mS/mm of gate width with a mobility μ_o = 4000 cm^2/V-sec. When μ_o = 1000 cm^2/V-sec, the g_m is reduced to 96.7 mS/mm of gate width. The drift mobility of the active layers was determined using a MESFET with a large gate length, "Fat FET". The "Fat FET" had a nominal gate length, L, of 50 microns which is much larger than drain-gate or source-gate spacings. This enables the resistance, R_c, due to the undepeleted region to make the dominant contribution. When a small source-drain potential, V_{ds}, compared to the external gate bias is applied, the depletion region is almost parallel to the interface

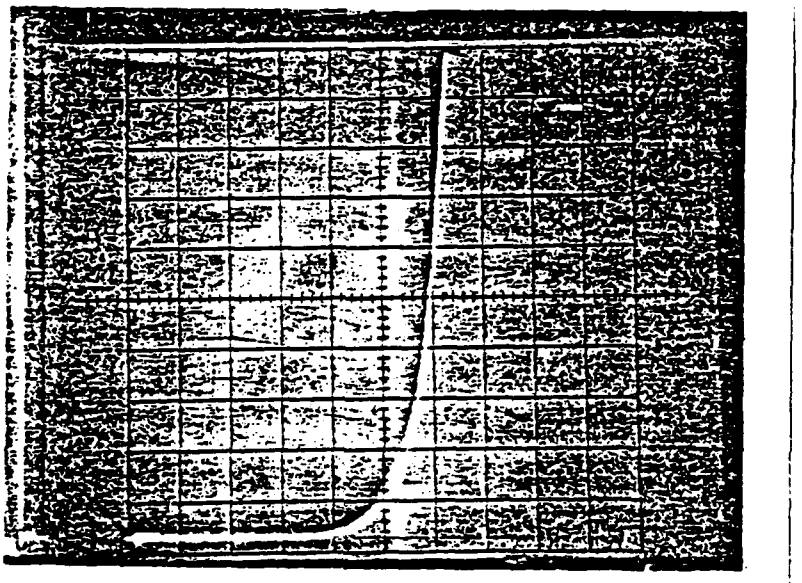
V_g = 0.5V/step



I_d = 2 mA/div

V_d = 0.5v/div

Figure 26: Source-drain I-V characteristics of 0.5 micron FET.



$I = 10\ A/div$

$V_g = 100\ mV/div$

Figure 27: I-V characteristics of gate of FET.

and the average longitudinal field is less than the peak threshold field. The drift mobility is given by

$$\mu_o(y)=(g_m/C_g)(L^2/V_{ds})(1/(1-(R_s+R_d)/R_T)^2)$$

where

$$R_T = R_s + R_d + R_c.$$

A capacitance versus voltage plot an doping profile plot were made. Transconductance was measured by applying a pulse to the gate and recording the change in channel current. Figure 28 is a plot of mobility versus distance.

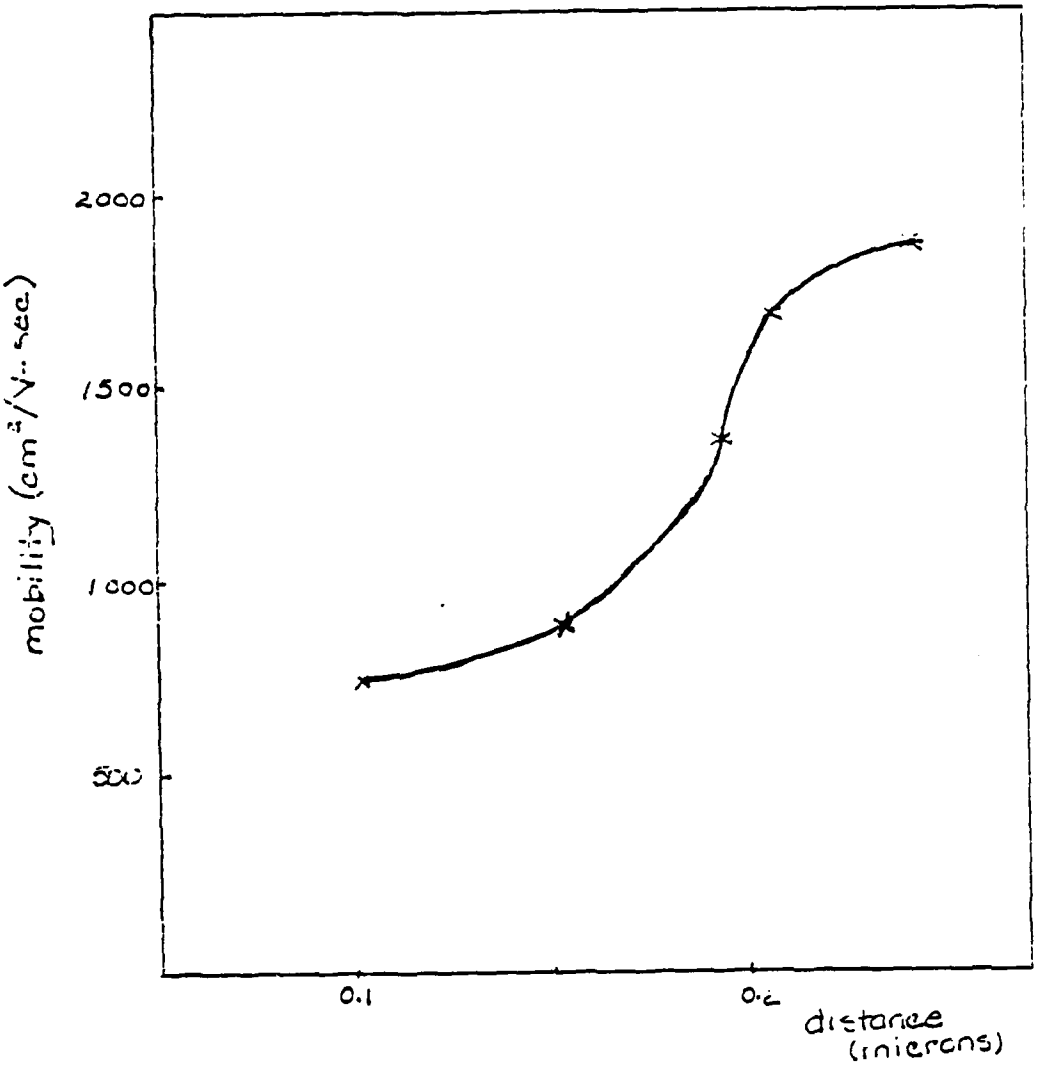


Figure 28: Drift Mobility vs. distance

CHAPTER V

DISCUSSION

This chapter discusses the results in Chapter IV and attempts to relate these results to conditions inherent to the fabrication process. We will also present work presently being carried out to circumvent particular problems.

The first thing to note here is the consistency in the measured parameters. The established process has maintained control of the gate length to a remarkable degree. Although we were inconsistent in reproducing 0.25 micron gates, 0.5 micron gates were achieved consistently each run. The 0.75 micron gates measured were not over developed 0.5 micron lines but actual resolutions of the mask.

The source and drain resistance values were relatively high, ranging from 41.0 to 68 ohms, and 11 to 42 ohms respectively. There are three possible causes for these high values. In examining the source/drain metallizations, there was a "balling-up" of the metal. At the edge of the mesa, there was a small area of contact because of the "balling-up" of the metal as it

went over the step. Also, close examination of the step showed that the mesa sloped inwards, so that the metal was not supported at the step and therefore easily broke as it went over the step. To eliminate that problem, we abandoned the slow mesa etch (200:1:1) and moved to a faster etch of a similar solution (40:1:1) of (H_2O:H_2O_2:NH_4OH). This etch produced an outward sloping mesa to support the metal over the step. We believe the "balling up" of the ohmics can be eliminated by the addition of nickel in the AuGe. Another cause for high R_S is due to possible diffusion of the gate metal into the channel during the alloying process. Our process, as it stands right now, alloys the ohmics with the gate in place opening the possibility of the gold on the gate to diffuse into the channel. Ideally, we would like to alloy the ohmic contacts before putting down the gate. However, alignment optics restrict us in aligning the gate between the source and drain. We are presently using titanium only as the gate metal in an effort to determine whether or not there is gold diffusion into the channel. At the time of writing this report, no devices had been completed so no results have been obtained.

The theory in Chapter II indicated the relationship of source resistance and transconductance; that is high values of R_S translate into lower values of transconductance. By definition, g_m is the change in channel current with respect to gate voltage. The parasitic source resistance serves as a limiter for the channel current and this is the reason why high R_S results in low values of transconductance. The results presented support this theory.

We anticipate that by creating a structure where the distance between the source and gate is reduced, the parasitic source resistance should decrease. In this structure the gate is put in place first, then a "T" structure is formed by selective etching of T_i in a freon plasma. After mesa definition: a blanket evaporation of AuGe follows. Source/drain pads are defined creating the structure shown in Figure 29. Our work, so far, has shown that with this process, it is possible to create devices with lines 0.3 microns and less.

Whereas the breakdown voltages of the devices are consistently high, the associated ideality factors for the Schottky barriers have been somewhat higher than

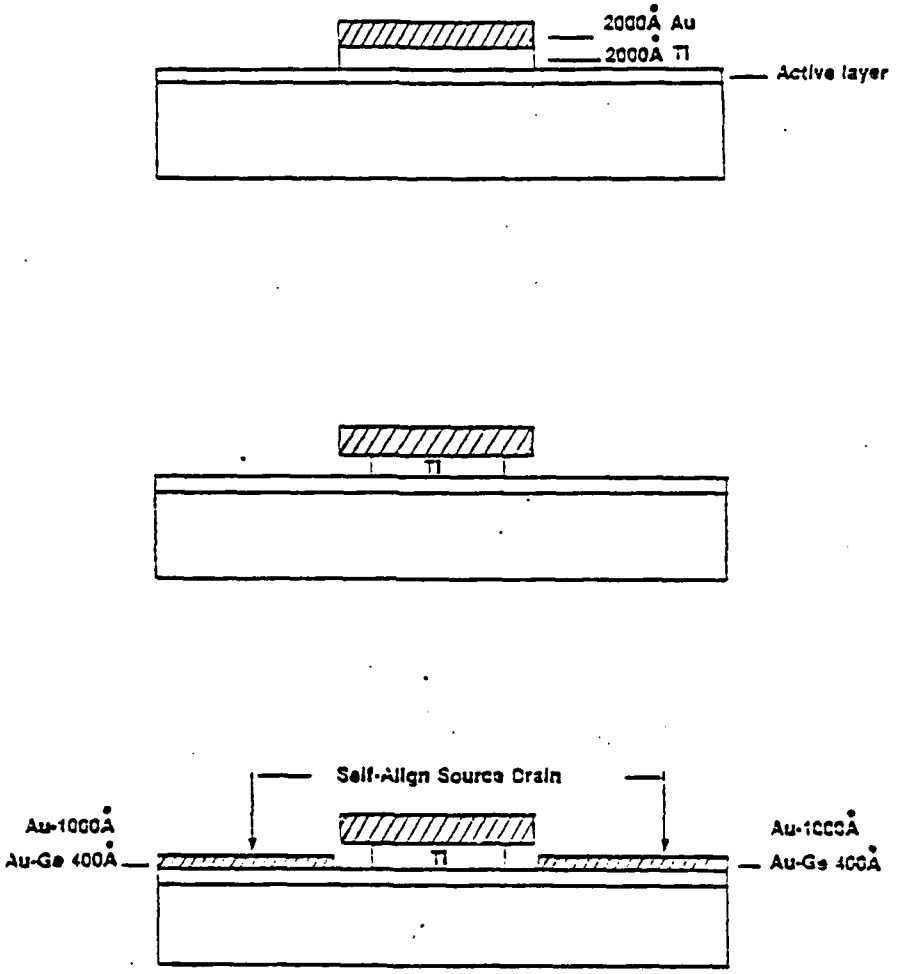


Figure 29: Self-aligned structure

expected. The measurements were taken at low values of current (in the micro amperes range). For high voltages at the gate, injection of carriers through the gate into the channel would occur reuslting in erroneous measurements of the ideality factor.

We found that the Schottky-barriers deteriorate during the alloying of the ohmic contacts. Metallic dots of Ti/Au were evaporated onto GaAs and ideality factor measurements were taken before and after alloying. The results indicated that the ideality factor did in fact increase by about 10 percent on the average after the dots were subjected to typical alloying temperatures.

The values recorded for g_m were low compared to reported values of 200 mS and greater. However, the consistently high parasitic source resistance and low drift mobility values are then considered to be the primary reasons for low g_m. This is supported by the theoretical calculations for g_m.

The values recorded for V_p are an indication of the active layer thickness. In some instances greater than 10 volts were needed to pinch-off the channel.

CHAPTER VI

CONCLUSION

The objective of this work was to fabricate and characterize a sub-micron MESFET using deep ultra violet contact lithography. We have been successful in this regard and can reproduce 0.5 micron lines consistently. The important parameters in achieving this resolution are quality of contact, exposure time, lamp intensity and development time. Another parameter extrinsic to the process but nonetheless just as important is humidity. Both PMMA and copolymer are sensitive to humidity and for humidity values of 55 percent or above, there is a drastic change in development times.

We believe deep ultra violet lithography can achieve resolutions down to 0.25 micron with the introduction of higher intensity lamps in the future or Excimer laser based instruments.

The results obtained from the devices fabricated were encouraging and did show that the deep UV is a viable process to produce 0.5 micron lines. Future

work in this area should experiment with thicker PMMA to achieve even better line-width control and a better "lift-off-lip".

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FIGURES

Figure 1: (a) Source and drain ohmic contacts
(b) Schottky Barrier Gate Reversed Biased. Drain voltage biased into velocity saturation at (C).

Figure 2: Drift velocity versus electric field for Si, GaAs and InP.

Figure 3: (a) Equivalent circuit of a GaAs MESFET and
(b) Physical origin of the circuit elements Figure 4: GaAs MESFET with velocity saturation.

Figure 5: Channel cross section, electric field, drift velocity and space-charge distribution in the channel of a GaAs MESFET operated in the current-saturation region (10).

Figure 6: Cross-sectional diagram of the idealized FET showing various geometrical dimensions and potentials used in the analysis. (a) Bias voltages, channel dimensions and reduced potentials. In the idealized model shown, parasitic resistances are absent, so that $V_{gs} = V_{gg}$ and $V_{ds} = V_{dd}$ (b) of channel (c) Potential distribution along symmetry plane. Also shown is gate bias potential and gate-to-channel potential.

Figure 7: Dependence of channel opening on normalized drain current for a special source-drain voltage and saturation parameters V_{ds}/W_{00} = 1, = 0.1.

Figure 8: Relative length of velocity-saturated region as a function of the normalized drain voltage and ratio L/a, I_d/I_s = 0.5, = 0.1.

Figure 9: Length of velocty-saturated region L_2 relative to epitaxial film thickness, a, as a function of the geometric ration L/a and . Drain voltage and drain current are held fixed, V_{ds}/W_{oo} = 1, I_d/I_s = 0.5.

Figure 10: A cross-sectional view of a GaAs MESFET.

Figure 11: (a) Gradual electron acceleration for GaAs MESFETs
(b) Electron velocity at the crystal limited velocity.

Figure 12: The forward I-V characteristics of an Aluminum gate diode at room temperature. The slope and the location of its linear poriton on a semi-log paper give the ideality parameter, n, and the gate built-in voltage, V_{bi}, respectively.

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Figure 16: Calibration of resist etch rate.

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Figure 18, 19, 20: Gate Metallization

Figure 21, 22: Scanning electron micro-graphs of completed FET calibration mark is one micron.

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Figure 26: Source-drain I-V characteristics of 0.5 micron FET.

Figure 27: Gate I-V characteristics.

Figure 28: Mobility versus distance.

Figure 29: Self-aligned device.

LIST OF TABLES

Table 1 Small-signal equivalent circuit elements.

Symbol	Definition	Effect on Performance
g_m	the transconductance of the MESFET = dI_D/dV_{GS} at constant V_{DS}	f_T is proportional to g_m increased electron velocity will increase g_m
R_{DS}	the drain resistance	f_{max} is proportional to the square root of R_{ds}
R_i	the input resistance	f_{max} is proportional to the square root of $1/R_i$
C_{GS}	THE SOURCE-GATE capacitance	f_T IS proportional to $1/C_{GS}$
C_{DG}	the drain-gate (or feedback) capacitance	f_{max} is proportional to the square root of $1/C_{DG}$
R_G	the gate metallization of the MESFET	f_{max} is proportional to the the square root of $1/R_G$
R_S	the source-gate capacitance	f_{max} is proportional to the square root of $1/R_S$
R_D	the drain resistance	
C_{DS}	the drain-source capacitance	

Table 2

Sample #	n	V_{bi}	V_{br}	Ps	P_n	V_p	ε_m	L_g
101	1.34	0.7	9	69.0	42.0	9	73.2	0.5
102	1.11	1.3	11.5	58.5	18.5	9.75	48.5	0.75
103	1.34	0.775	9	42.25	34.25	12.5	64.7	0.6
104	1.17	0.9	11	38	34	8.5	65	0.5
105	1.11	0.92	10.5	42	34	11.5	64.2	0.5
106	2.02	0.64	10	56	11	12	58.1	0.6
107	1.17	0.75	6.5	41	14	8.5	68.4	0.75
108	1.34	0.675	7.5	65	11	8	72.0	0.5
109	1.15	0.91	9	45	15	9.2	53.2	0.75
110	1.01	0.84	10.3	53	18	10.5	55.9	0.5

Interactions

The work on the annealing of undoped GaAs sparked interest and resulted in several seminars by one of the principal investigators or his graduate student M. Asom. These seminars were given at Bell Laboratories (Murray Hill), IBM (Thomas J. Watson) and Cornell.

During the course of this contract there have been several consultant activities both formal and informal, these activities are listed below:

1. Naval Research Laboratories We colaborted on work involving deep levels in ion implanted GaAs This was a study which tried to determine the limitations of ion implantation particularly with respect to the production of deep levels. The study was conducted with epitaxial MBE or LPE material. In this study Dr. M. G. Spencer has interacted with Drs. H. Dietrich and R. Magno.

2. Lawrence Livermore Laboratories We advised on the materials considerations in fabricating GaAs integrated circuits. Also provided MBE epitaxial material. We interacted with Drs. Paul Phelps and Steve Swierkowski.

3. Harry Diamond Laborary We have informally advised on GaAs materials issues and provided epitaxial material. We interacted with Dr. George Simmonis.

Professional Personnel

Principal Investigators

Dr. M.G. Spencer

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Technical Staff

James Griffen	Research Associate
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Graduate Students

Marie Wray	"Fabrication and Characterization of GaAs Mesfets" completion date of Masters Thesis May 1935
Leary Myers	"Fabrication and DC Characterization of the sub-micron field effect transistor using deep ultra violet radiation" completion date of Masters Thesis December 1934
Moses Asom	"A study of III-V Semiconductor Processing Employing High Purity Epitaxial Gallium Arsenide" completion date of Phd. Thesis November 1935